WHAT IS CLAIMED IS:

1. A semiconductor memory apparatus comprising:

a memory unit having unit blocks each including:

a memory core including a plurality of memory cells laid out to form a cell matrix; and

redundant lines including redundant memory cells each used for repairing an abnormal memory cell generated in any of said memory cores,

wherein:

said unit blocks are further laid out to form a block matrix or a plurality of block matrixes, and every plurality of said unit blocks forms a two-dimensional group oriented in a first direction (row or column direction) and a second direction (column or row direction); and

said redundant lines are shared by said unit blocks pertaining to said two-dimensional group in both said first and second directions;

self-test means mounted in the same chip as said memory unit to serve as embedded self-test means for evaluating said memory cells in order to determine whether said memory cells are good or defective; and

self-repair means mounted in said same chip as said memory unit to serve as embedded self-repair means for:

selecting only a minimum number of address pairs among address pairs received from said self-test means as address pairs each comprising a first-direction address (row or column address) and second-direction address (column or row address) of an abnormal memory cell;

storing said selected minimum number of address pairs in storage means provided for each of said unit blocks as address pairs required for determining a redundant line to be used for repairing an abnormal memory cell; and

finding a redundant line to be used for repairing an abnormal memory cell for each of said unit blocks pertaining to said two-dimensional group on the basis of address pairs stored in said storage means.

2. A semiconductor memory apparatus according to claim 1 wherein said embedded self-repair means comprises:

first confirmation means for determining whether or not it is possible to repair an abnormal memory cell in each of said unit blocks pertaining to each of second-direction one-dimensional subgroups composing said two-dimensional group; and

second confirmation means for reflecting a

determination result produced by said first confirmation means for any particular one of said second-direction one-dimensional subgroups in said unit blocks pertaining to any other one of said second-direction one-dimensional subgroups, which is provided at a location separated away in said first direction from said particular second-direction one-dimensional subgroup, and determining whether or not it is possible to repair an abnormal memory cell in each of said unit blocks pertaining to said other second-direction one-dimensional subgroup.

3. A semiconductor memory apparatus according to claim 2 wherein said embedded self-repair means has an address notification line for reporting information on a first-direction address determined to be repairable by said first confirmation means from any particular one of said second-direction one-dimensional subgroups to any other one of said second-direction one-dimensional subgroups, which is provided at a location separated away in said first direction from said particular second-direction one-dimensional subgroup.

4. A semiconductor memory apparatus according to claim 3 wherein said address notification line comprises as many address buses as said redundant lines connected in said first direction and usage bit lines for

indicating states of utilization of said address buses.

5. A semiconductor memory apparatus according to claim 3 wherein said address notification line comprises an address bus, usage bit lines for indicating the number of currently used redundant lines connected in said first direction and select bit lines for indicating which redundant line connected in said first direction has an address thereof appearing on said address bus.

6. A self-repair method adopted in a semiconductor memory apparatus comprising:

a memory unit having unit blocks each including:

a memory core including a plurality of memory cells laid out to form a cell matrix; and

redundant lines including redundant memory cells each used for repairing an abnormal memory cell generated in any of said memory cores,

wherein:

said unit blocks are further laid out to form a block matrix or a plurality of block matrixes, and every plurality of said unit blocks forms a two-dimensional group oriented in a first direction (row or column direction) and a second direction (column or row direction); and

said redundant lines are shared by said unit

blocks pertaining to said two-dimensional group in both said first and second directions; and

self-test means mounted in the same chip as said memory unit to serve as embedded self-test means for evaluating said memory cells in order to determine whether said memory cells are good or defective,

said self-repair method comprising:

a storage process of storing address pairs each consisting a first-direction address (a row address or a column address) and second-direction address (column address or row address) of an abnormal memory cell in storage means provided for each of said unit blocks;

a first confirmation process of determining whether or not it is possible to repair an abnormal memory cell in each of said unit blocks sharing said redundant lines connected in said second direction and pertaining to any particular one of second-direction one-dimensional subgroups composing said two-dimensional group on the basis of address pairs stored in said storage means in said storage process; and

a second confirmation process of reflecting a determination result produced in said first confirmation process for any particular one of said second-direction one-dimensional subgroups in said unit blocks pertaining

to any other one of said second-direction one-dimensional subgroups, which is provided at a location separated away in said first direction from said particular second-direction one-dimensional subgroup, and determining whether or not it is possible to repair an abnormal memory cell in each of said unit blocks pertaining to said other second-direction one-dimensional subgroup,

whereby said first and second confirmation processes are carried out repeatedly to determine whether or not it is possible to repair an abnormal memory cell in each of said unit blocks pertaining to said two-dimensional subgroup.

7. A self-repair method according to claim 6 wherein said first confirmation process comprises:

a first sub-process of generating a pattern of an address set of a second-direction address on the basis of an address pair stored in said storage means for said unit blocks pertaining to said particular second-direction one-dimensional subgroup;

a second sub-process of regarding said generated address set of said second-direction address as a repair address, reporting said address set to all said unit blocks pertaining to said particular second-direction one-dimensional subgroup and determining whether or not

it is possible to repair the address pair of an abnormal memory cell, which cannot be repaired by said address set, by using any one of said redundant lines connected in said first direction for all said unit blocks pertaining to said particular second-direction one-dimensional subgroup; and

a third sub-process of generating a next address set to be used for determining whether or not it is possible to repair the address pair of an abnormal memory cell for all said unit blocks pertaining to said particular second-direction one-dimensional subgroup if a result of said second sub-process indicates that the address pair of an abnormal memory cell is left in an unrepairable state in any of said unit blocks pertaining to said particular second-direction one-dimensional subgroup,

whereby said sub-processes are carried out repeatedly to determine second-direction repair addresses.

8. A self-repair method according to claim 6 wherein, on the assumption that said second-direction one-dimensional subgroups are named a first subgroup, a second subgroup, a third subgroup --- and a Nth subgroup, said second confirmation process comprises the steps of:

finding an address set of a second-direction repair

address in said first subgroup by applying an algorithm adopted in said first confirmation process to said unit blocks pertaining to said first subgroup;

determining a plurality of candidates for an address set of a first-direction repair address in said first subgroup on the basis of said address set of a second-direction repair address in said first subgroup, reporting one of said candidates to said second subgroup and finding an address set of a second-direction repair address in said second subgroup by taking an effect of said reported candidate into consideration;

determining a plurality of candidates for an address set of a first-direction repair address in said second subgroup on the basis of said address set of a second-direction repair address in said second subgroup, reporting one of said candidates and said address set of a first-direction repair address in said first subgroup to said third subgroup and finding an address set of a second-direction repair address in said third subgroup by taking an effect of said reported candidate and said address set of a first-direction repair address in said first subgroup into consideration; and

executing said above step thereafter repeatedly till said Nth subgroup is reached to determine a first-

direction repair address and a second-direction repair address for each of said subgroups.

9. A self-repair method according to claim 8 whereby, if the number of first-direction repair addresses exceeds the number of redundant lines connected in said second direction in the course of an operation carried out as part of said second confirmation process to determine first-direction repair addresses and second-direction repair addresses for all said second-direction one-dimensional subgroups, an unrepairable state is determined and, if a repairable pattern is not found in a particular one of said second-direction one-dimensional subgroups, said second confirmation process is repeated by starting from a previous one of said second-direction one-dimensional subgroups, which immediately precedes said particular second-direction one-dimensional subgroup, to further find a next address set in said immediately preceding second-direction one-dimensional subgroup.

10. A self-repair method according to claim 8 whereby, in said second confirmation process, first-direction repair addresses reported to the (n + 1)th subgroup as first-direction repair addresses of the first to nth subgroups are also reported to the (n + 2)th and subsequent subgroups at the same time or also reported to

all said subgroups at the same time where $2 < n < N$.

11. A self-repair method according to claim 8 whereby, in said second confirmation process:

first-direction repair addresses reported to the (n + 1)th subgroup as first-direction repair addresses of the first to nth subgroups are also reported to the (n + 2)th and subsequent subgroups at the same time or also reported to all said subgroups at the same time where $2 < n < N$; and

if an address pair having a first direction address matching any one of said reported first-direction repair addresses is found in said storage means, said address pair is assumed to be a repaired address pair.

12. A self-repair method according to claim 11 whereby, in an operation carried out as part of said second confirmation process to assume an address pair to be a repaired address pair, a special bit provided for each of address pairs storable in said storage means is set to indicate that an address pair associated with said set special bit has been assumed to be a repaired address pair.

13. A self-repair method according to claim 8 whereby, in an operation carried out as part of said second confirmation process to determine a second-

direction repair address in the nth subgroup by applying an algorithm adopted by said first confirmation process where n has a value in the range 1 to N, first-direction repair addresses reported from other ones of said nth subgroup are taken into consideration.